

# M5L2764K, -2

**65536-BIT (8192-WORD BY 8-BIT)  
ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM**

## DESCRIPTION

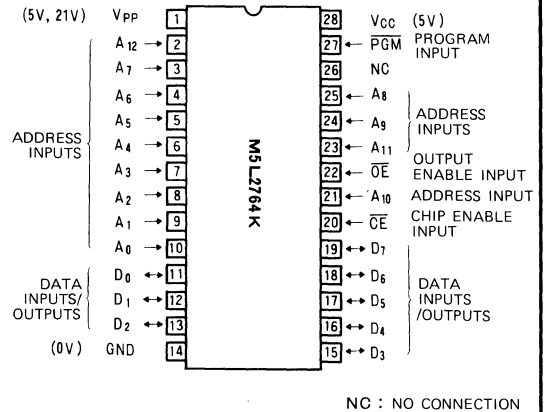
The Mitsubishi M5L2764K is a high-speed 65536-bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5L2764K is fabricated by N-channel double polysilicon gate technology and is available in a 28-pin DIL package with a transparent lid.

## FEATURES

- 8192 Word x 8-bit Organization
- Access Time  

M5L2764K-2	200 ns (Max)
M5L2764K	250 ns (Max)
- Two Line Control  $\overline{OE}$ ,  $\overline{CE}$
- Low Power Current ( $I_{CC}$ ) Active . . . . . 150 mA (Max)  
 Standby . . . 35 mA (Max)
- Single 5V Power Supply
- 3-State Output Buffer
- Input and Output TTL-Compatible in Read and Program Mode
- Standard 28-pin DIL Package
- Single Location Programming with One 50 ms Pulse
- Fast programming algorithm
- Interchangeable with INTEL 2764

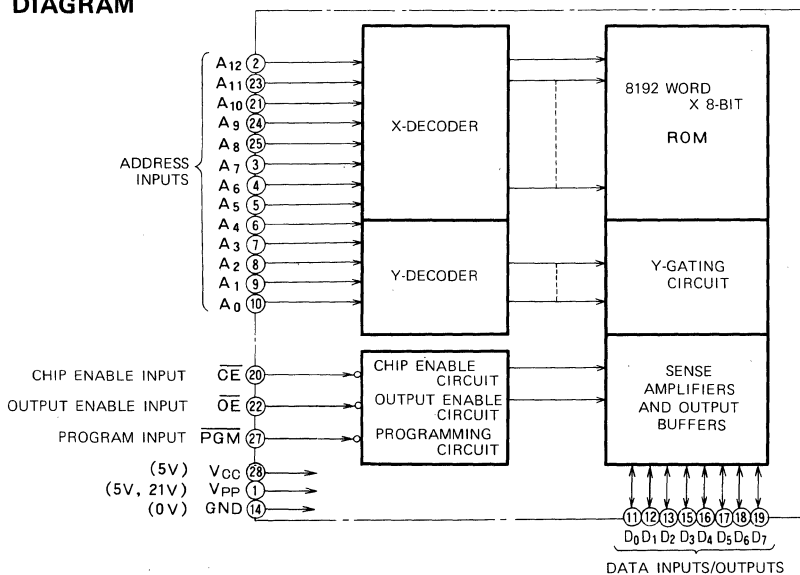
## PIN CONFIGURATION (TOP VIEW)



Outline 28K1

NO : NO CONNECTION

## BLOCK DIAGRAM



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**FUNCTION**

**Read**

Set the  $\overline{CE}$  and  $\overline{OE}$  terminals to the read mode (low level). Low level input to  $\overline{CE}$  and  $\overline{OE}$  and address signals to the address inputs ( $A_0 \sim A_{12}$ ) make the data contents of the designated address location available at the data input/output ( $D_0 \sim D_7$ ). When the  $\overline{CE}$  or  $\overline{OE}$  signal is high, data input/output are in a floating state.

When the  $\overline{CE}$  signal is high, the device is in the standby mode or power-down mode.

In the read mode  $V_{PP}$  must be at  $V_{CC}$  level.

**Programming  
 (Fast programming algorithm)**

First set  $V_{CC}=6V$ ,  $V_{PP}=21V$  and then set an address to first address to be programmed. After applying 1 ms program pulse (PGM) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 1 ms program pulse. The programmer continues 1 ms pulse-then-verify routines until the device verify correctly or fifteen of these pulse-then-verify routines have been completed. The programmer also maintains its total number of 1 ms pulses applied to that address in register X. And then applied a program pulse 4 times of register X value long as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed. (See P.6-9)

**(Conventional programming algorithm)**

The device enters the programming mode when 21V is supplied to the  $V_{PP}$  power supply input and  $\overline{CE}$  is at low level. A location is designated by address signals ( $A_0 \sim A_{12}$ ), and the data to be programmed must be applied at 8-bits in parallel to the data inputs ( $D_0 \sim D_7$ ). A program pulse to the PGM at this state will effect programming. Only one programming pulse is required, but its width must satisfy the condition  $45 \text{ ms} \leq t_{PW} \leq 55 \text{ ms}$ .

**Erase**

Erase is effected by exposure to ultraviolet light with a wavelength of 2537Å at an intensity of approximately 15WS/cm<sup>2</sup>. Sunlight and fluorescent light may contain ultraviolet light sufficient to erase the programmed information. For any operation in the read mode, the transparent lid should be covered with opaque tape.

**MODE SELECTION**

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	PGM(27)	$V_{PP}$ (1)	$V_{CC}$ (28)	Outputs (11~13, 15~19)
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{CC}$	$V_{CC}$	Data out
Standby	$V_{IH}$	X*	X*	$V_{CC}$	$V_{CC}$	Floating
Program	$V_{IL}$	X*	$V_{IL}$	$V_{PP}$	$V_{CC}$	Data in
Program verify	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{PP}$	$V_{CC}$	Data out
Program inhibit	$V_{IH}$	X*	X*	$V_{PP}$	$V_{CC}$	Floating

\*: X can be either  $V_{IL}$  or  $V_{IH}$ .

**ABSOLUTE MAXIMUM RATINGS (Note 1)**

Symbol	Parameter	Limits	Unit
$T_{opr}$	Temperature under bias	-10 ~ 80	°C
$T_{stg}$	Storage temperature	-65 ~ 125	°C
$V_{I1}$	All input or output voltage (Note 2)	-0.6 ~ 7	V
$V_{I2}$	$V_{PP}$ supply voltage during programming (Note 2)	-0.6 ~ 26.5	V

Note 1: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

2: With respect to Ground.

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**READ OPERATION**

$T_a = 0^\circ$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 5\%$ ,  $V_{PP} = V_{CC}$

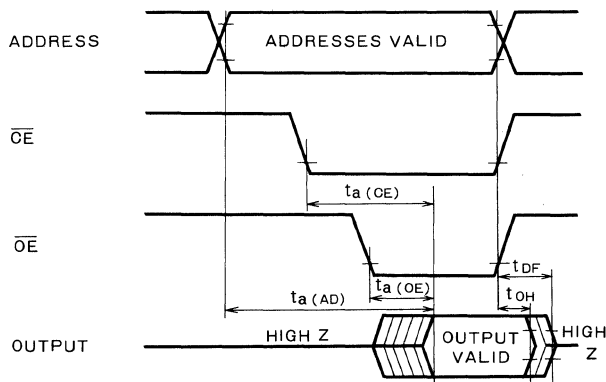
**D. C. CHARACTERISTICS**

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$I_{LI}$	Input load current	$V_{IN} = 5.25V$			10	$\mu\text{A}$
$I_{LO}$	Output leakage current	$V_{OUT} = 5.25V$			10	$\mu\text{A}$
$I_{PP1}$	$V_{PP}$ current read	$V_{PP} = 5.25V$			15	mA
$I_{CC1}$	$V_{CC}$ current standby	$\overline{CE} = V_{IH}$			35	mA
$I_{CC2}$	$V_{CC}$ current active	$\overline{CE} = \overline{OE} = V_{IL}$			150	mA
$V_{IL}$	Low-level input voltage		-0.1		0.8	V
$V_{IH}$	High-level input voltage		2.0		$V_{CC} + 1$	V
$V_{OL}$	Low-level output voltage	$I_{OL} = 2.1\text{mA}$			0.45	V
$V_{OH}$	High-level output voltage	$I_{OH} = -400\mu\text{A}$	2.4			V

**A. C. CHARACTERISTICS**

Symbol	Parameter	Test conditions	M5L2764K-2		M5L2764K		Unit
			Min	Max	Min	Max	
$t_a$ (AD)	Address to output delay	$\overline{CE} = \overline{OE} = V_{IL}$		200		250	ns
$t_a$ (OE)	$\overline{CE}$ to output delay	$\overline{OE} = V_{IL}$		200		250	ns
$t_a$ (OE)	Output enable to output delay	$\overline{CE} = V_{IL}$	10	70	10	100	ns
$t_{DF}$	Output enable high to output float	$\overline{CE} = V_{IL}$	0	60	0	90	ns
$t_{OH}$	Output hold from $\overline{CE}$ or $\overline{OE}$	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		ns

**AC WAVEFORMS**



Test Conditions for A.C. Characteristics

Input Voltage:  $V_{IL} = 0.8V$ ,  $V_{IH} = 2.2V$

Input Rise and Fall Times:  $\leq 20\text{ns}$

Reference Voltage at Timing Measurement:

Inputs 1V and 2V

Outputs 0.8V and 2V

Output Load: 1 TTL gate,  $C_L = 100\text{pF}$

**CAPACITANCE** ( $T_a = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$ )

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$C_{IN}$	Input capacitance	$V_{IN} = 0V$		4	6	pF
$C_{OUT}$	Output capacitance	$V_{OUT} = 0V$		8	12	pF

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**PROGRAM OPERATION**

**CONVENTIONAL PROGRAMMING ALGORITHM** ( $T_a = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 5V \pm 5\%$ ,  $V_{PP} = 21 \pm 0.5V$  unless otherwise noted)

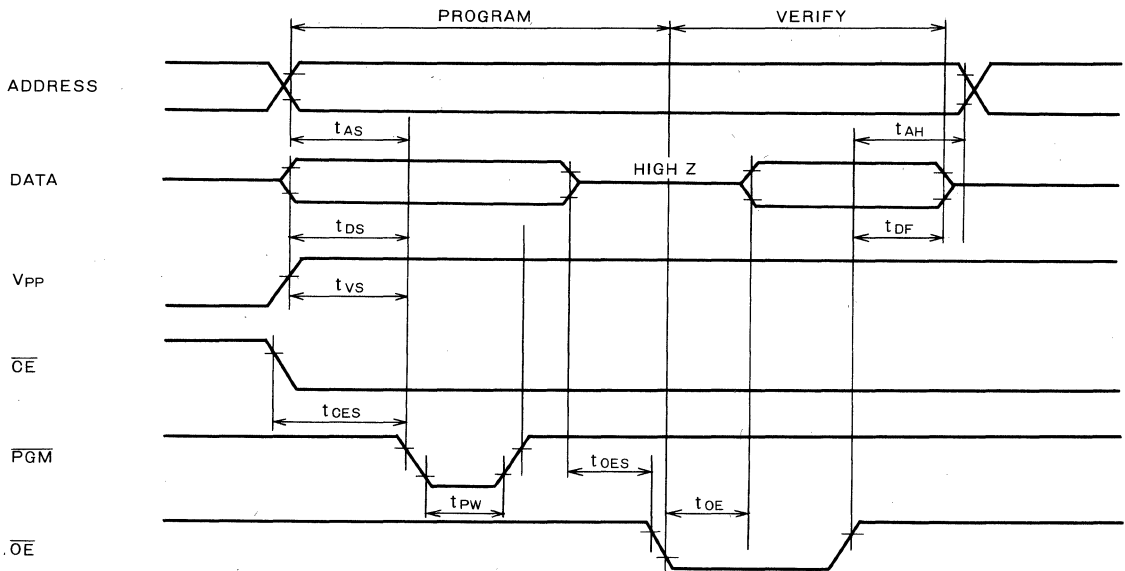
**D. C. CHARACTERISTICS**

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$I_{LI}$	Input current	$V_{IN} = V_{IL}$ or $V_{IH}$			10	$\mu\text{A}$
$V_{OL}$	Low-level output voltage (verify)	$I_{OL} = 2.1\text{mA}$			0.45	V
$V_{OH}$	High-level output voltage (verify)	$I_{OH} = -400\mu\text{A}$	2.4			V
$I_{CC2}$	$V_{CC}$ supply current (active)				100	mA
$V_{IL}$	Low-level input voltage		-0.1		0.8	V
$V_{IH}$	High-level input voltage		2.0		$V_{CC} + 1$	V
$I_{PP}$	$V_{PP}$ supply current	$\overline{CE} = V_{IL} = \overline{PGM}$			30	mA

**A. C. CHARACTERISTICS**

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{AS}$	Address setup time		2			$\mu\text{s}$
$t_{OES}$	$\overline{OE}$ setup time		20			$\mu\text{s}$
$t_{DS}$	Data setup time		2			$\mu\text{s}$
$t_{AH}$	Address hold time		0			$\mu\text{s}$
$t_{DH}$	Data hold time		2			$\mu\text{s}$
$t_{DF}$	Chip enable to output delay		0		130	ns
$t_{VS}$	$V_{PP}$ setup time		2			$\mu\text{s}$
$t_{PW}$	$\overline{PGM}$ pulse width (programming)		45	50	55	ms
$t_{CES}$	$\overline{CE}$ setup time		2			$\mu\text{s}$
$t_{OE}$	Data valid from $\overline{OE}$				150	ns

**AC WAVEFORMS**



Test Conditions for AC Characteristics  
 Input Voltage:  $V_{IL} = 0.8V$ ,  $V_{IH} = 2.2V$   
 Input Rise and Fall Times:  $\leq 20\text{ns}$   
 Reference Voltage at Timing Measurement: Inputs 1V and 2V  
 Outputs 0.8V and 2V

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**ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM**

**FAST PROGRAMMING ALGORITHM**

**DC CHARACTERISTICS** ( $T_a = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6V \pm 0.25V$ ,  $V_{PP} = 21V \pm 0.5V$ , unless otherwise noted)

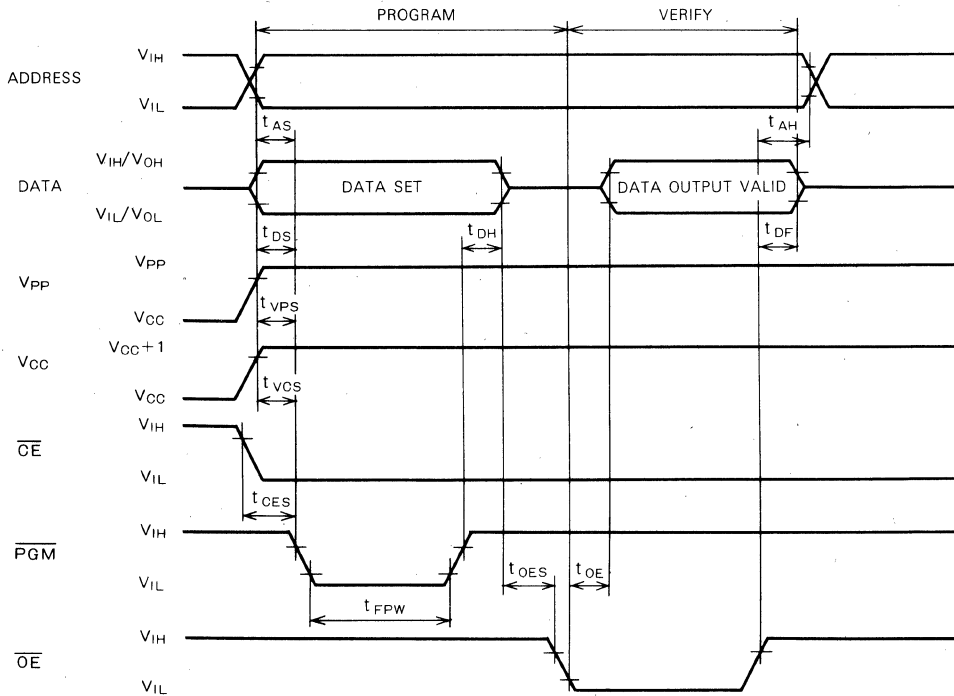
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$I_{LI}$	Input current	$V_{IN} = V_{IL}$ or $V_{IH}$			10	$\mu\text{A}$
$V_{OL}$	Output low voltage	$I_{OL} = 2.1\text{mA}$			0.45	V
$V_{OH}$	Output high voltage	$I_{OH} = -400\mu\text{A}$	2.4			V
$V_{IL}$	Input low voltage		-0.1		0.8	V
$V_{IH}$	Input high voltage		2.0		$V_{CC}$	V
$I_{CC2}$	$V_{CC}$ supply current				100	mA
$I_{PP2}$	$V_{PP}$ supply current	$\overline{CE} = V_{IL} = \overline{PGM}$			30	mA

**AC CHARACTERISTICS** ( $T_a = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6V \pm 0.25V$ ,  $V_{PP} = 21V \pm 0.5V$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{AS}$	Address setup time		2			$\mu\text{s}$
$t_{OES}$	$\overline{OE}$ set up time		20			$\mu\text{s}$
$t_{DS}$	Data setup time		2			$\mu\text{s}$
$t_{AH}$	Address hold time		0			$\mu\text{s}$
$t_{DH}$	Data hold time		2			$\mu\text{s}$
$t_{DF}$	Chip enable to output float delay		0		130	ns
$t_{VCS}$	$V_{CC}$ setup time		2			$\mu\text{s}$
$t_{VPS}$	$V_{PP}$ setup time		2			$\mu\text{s}$
$t_{FPW}$	$\overline{PGM}$ initial program pulse width		0.95	1	1.05	ms
$t_{OPW}$	$\overline{PGM}$ over program pulse width		3.8		63	ms
$t_{CES}$	$\overline{CE}$ setup time		2			$\mu\text{s}$
$t_{OE}$	Data valid from $\overline{OE}$				150	ns

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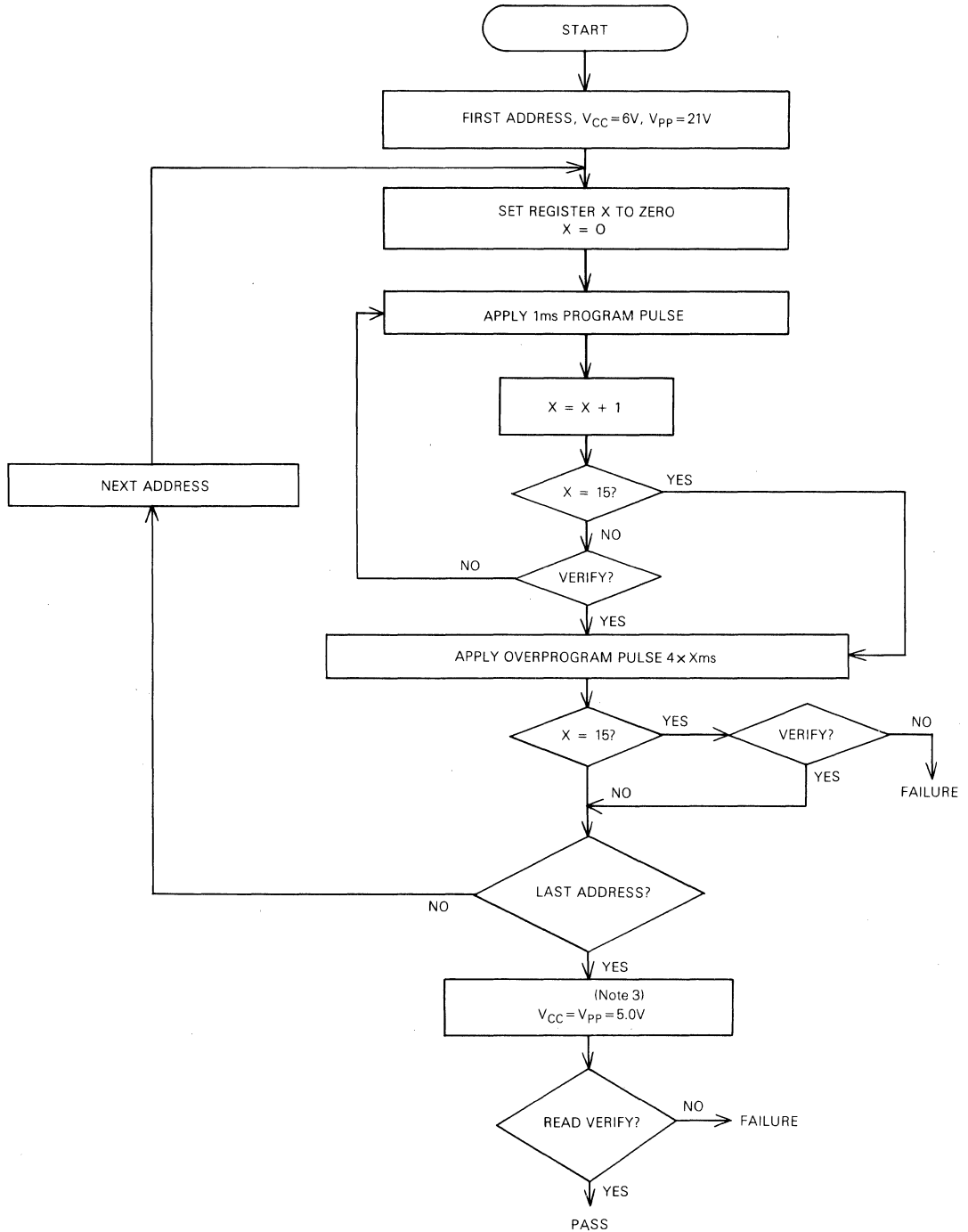
**AC WAVEFORMS**



Test conditions for A.C. characteristics  
 Input voltage:  $V_{IL}=0.8V$ ,  $V_{IH}=2.2V$   
 Input rise and fall times:  $\leq 20ns$   
 Reference voltage at timing measurement: Input 1V and 2V Output 0.8V, and 2V

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**FAST PROGRAMMING ALGORITHM  
 FLOW CHART**



Note 3:  $4.75 \leq V_{CC} = V_{PP} \leq 5.25V$